CLAIMS:

1. A method for testing integrated circuits having a plurality of field-effect transistors (FETs) of low threshold voltages, comprising the following steps:

determining at least one circuit cell (12, 13; 22, 23; 32, 33) to be tested in said integrated circuit;

separating said circuit cell (12, 13; 22, 23; 32, 33) into two independent cell networks;

obtaining a first response sequence for the first (12; 22; 32) of said two independent cell networks;

obtaining a second response sequence for the second of (13; 23; 33) said two independent cell networks, and

processing the first response sequence and the second response sequence in order to detect a defect in said circuit cell.

2. The method according to claim 1, wherein the step of processing comprises a step of comparing the first response sequence with the second response sequence to detect an inconsistency.

3. The method according to claim 1, wherein the step of processing comprises a step of comparing the first response sequence and the second response sequence with a sequence of expected responses to detect an inconsistency.

4. The method according to claim 1, comprising:

powering up said circuit cell (CMOS or BiCMOS);

selecting p- (12; 22; 32) and n-channel (13; 23; 33) transistor networks in said circuit cell;

putting said circuit cell (CMOS or BiCMOS) into a test mode whereby the p- and n-channel transistor networks in said circuit cell are stimulated by a sequence of test vectors;

obtaining a sequence of actual responses from said p-channel transistor network;

obtaining a sequence of actual responses from said n-channel transistor network;

determining whether a defect is detected in said circuit cell, wherein said step of detection is either based upon an inconsistency between said two sequences of actual responses or upon an inconsistency between said two sequences of actual responses and a sequence of expected responses.

5. The method of claim 1 or 4, wherein means (14, 15; 24, 25; 34, 35) are used to electrically separate said circuit cell into the first (12; 22; 32) of said two independent cell networks and the second (13; 23; 33) of said two independent cell networks.

6. The method of one of the claims 1 to 5, wherein load means (16, 17; 26, 27; 36, 37) are used which act as loads for said two independent cell networks (12, 13; 22, 23; 32, 33) while at least said cell of the integrated circuit to be tested is in test mode.

7. The method of claim 6, further comprising:

measuring the current drain of the circuit cell;

determining whether a defect is detected in said load means wherein said step of detection is based upon the amount of said current drain when said circuit cell has reached a predetermined quiescent state.

8. The method of one of the claims 4 to 7, comprising the additional step:

suppressing leakage currents in said circuit cell by turning off one or more of said control means while said circuit cell is in standby mode.

9. Integrated circuit including testing circuitry, comprising at least one circuit cell (12, 13; 22, 23; 32, 33), means (14, 15; 24, 25; 34, 35) to electrically separate said circuit cell into a first cell network (12; 22; 32) and a second cell network (13; 23; 33), and at least one output giving a first response sequence for the first of said two independent cell networks and a second response sequence for the second of said two independent cell networks.

10. The integrated circuit of claim 9, wherein the first cell network is a p-channel transistor network (12) and the second cell network is an n-channel transistor network (13).

11. The integrated circuit of claim 9 or 10, comprising control circuitry (14, 15; 24, 25; 34, 35) to deactivate said p- and n-channel transistor networks (12, 13; 22, 23; 32, 33) or to electrically separate them from each other, and wherein said control circuitry is connected in series with said n- and p-channel transistor networks.

12. The integrated circuit of claim 10 or 11, further comprising load means (16, 17; 26, 27; 36, 37) which act as loads for said p- and n-channel transistor networks while said network (12, 13; 22, 23; 32, 33) is in test mode.

13. The integrated circuit of one of the claims 10, 11, or 12, comprising connection circuitry (38, 39) connecting electrical signals of the control circuitry (34, 35) to other subcircuits for the purpose of testing them by selectively turning on or off said control circuitry and/or said load means (36, 37).